IN THE CLAIMS

Please cancel claims 33 and 35-63. All pending claims and status indicators have been reproduced below.

1. (previously amended) A system comprising:

a processor; and

a memory device operatively coupled to the processor, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of non-metal mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips physically coupled to a respective one of the plurality of packages.

2. (canceled)

3. (previously amended) The system, as set forth in claim 1, wherein each package comprises:

a molded resin body having a die side and a ball side.

4. (previously amended) The system, as set forth in claim 3, wherein each package comprises:

a plurality of first mateable alignment features on the die side of the package; and

a plurality of second mateable alignment features on the ball side of the package.

5. (previously amended) The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

6. (previously amended) The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

7. (previously amended) The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

8. (previously amended) The system, as set forth in claim 4, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

9. (previously amended) The package, as set forth in claim 4, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

10. (previously amended) The package, as set forth in claim 9, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

11. (previously amended) The package, as set forth in claim 9, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

12. (previously amended) The package, as set forth in claim 4, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.

13. (previously amended) The system, as set forth in claim 1, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

14. (original) The system, as set forth in claim 13, wherein each of the plurality of packages comprise vias extending therethrough to connect solder balls of adjacent packages serially.

15. (previously amended) A memory board comprising:

a substrate; and

a memory device operatively coupled to the substrate, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of non-metal mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

16. (original) The memory board as set forth in claim 15, wherein the substrate is a printed circuit board.

17. (original) The memory board, as set forth in claim 15, further comprising a memory controller operatively coupled to the memory device and to the substrate.

18. (canceled)

19. (previously amended) The memory board, as set forth in claim 15, wherein the package comprises:

a molded resin body having a die side and a ball side.

20. (previously amended) The memory board, as set forth in claim 19, wherein the molded resin package comprises:

a plurality of first mateable alignment features on the die side of the package; and

a plurality of second mateable alignment features on the ball side of the package.

21. (previously amended) The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are female.

22. (previously amended) The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are male and the plurality of second mateable alignment features are male.

23. (previously amended) The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are male.

24. (previously amended) The memory board, as set forth in claim 20, wherein the plurality of first mateable alignment features are female and the plurality of second mateable alignment features are female.

25. (previously amended) The package, as set forth in claim 20, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features orient adjacent packages in a unique location.

26. (previously amended) The package, as set forth in claim 25, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features are arranged asymmetrically.

27. (previously amended) The package, as set forth in claim 25, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features comprising of at least one unique alignment feature.

28. (previously amended) The package, as set forth in claim 20, wherein the plurality of first mateable alignment features and the plurality of second mateable alignment features support adjacent packages during solder ball reflow.

29. (previously amended) The memory board, as set forth in claim 15, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

30. (original) The memory board, as set forth in claim 29, wherein each of the plurality of packages comprise vias extending therethrough to connect solder balls of adjacent packages serially.

31. (original) The memory board, as set forth in claim 15, wherein a first ball grid array is coupled to a second ball grid array.

32. (original) The memory board, as set forth in claim 15, wherein the first ball grid array is serially coupled to the second ball grid array.

33-63. (canceled)